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|  | 16-bit Five Stage MIPS Processor |
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|  | Jared Mann V00187636, Taylor Long V00862856  CENG 450: Computer Systems and Architecture  3/30/17 |

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# Objective

## Abstract

Modern processors implement pipelining to increase throughput. Many current processors implement pipelining with various stage depths having more than 5 stages such as Intel, AMD, and even current ARM processors. Pipelining is a standard across all modern architecture designs.

## Project Objective

Build a synthesizable 5-stage 16-bit RISC processor; use VHDL to describe the processor, and Xilinx to synthesize and implement the design on a Spartan 3E FPGA.

# Design Requirement

## Instruction Set

The processor must handle three types of instructions:

* A-Format (arithmetic instructions)
* B-Format (branch instructions)
* L-Format (load and store instructions)

Regarding these types of instructions, the processor must be able to execute any program written using this instruction set.

# System

# Individual Module Design

# Simulation Result

# Analysis and Discussion

# Conclusion

# Appendices

# References