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|  | 16-bit Five Stage MIPS Processor |
|  |  |
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# Objective

## Abstract

Modern processors implement pipelining to increase throughput. Many current processors implement pipelining with various stage depths having more than 5 stages such as Intel, AMD, and even current ARM processors. Pipelining is a standard across all modern architecture designs.

## Project Objective

Build a processor; using VHDL to describe the processor, and Xilinx to synthesize and implement the design on a Spartan 3E FPGA.

# Design Requirement

## General Design Requirements

### Instruction Set

The project must implement a 16-bit RISC-like instruction set. Following the format outlined on the lab website. (Dimopolous & Hazmi, 2017) The instructions are all 1-word long.

The processor must handle three types of instructions:

* A-Format (arithmetic instructions)
* B-Format (branch instructions)
* L-Format (load and store instructions)

### Registers and Memory

Registers and Memory require certain implementations:

* 8 16-bit general purpose registers, each 1-word long, with word alignment.
* A memory address space that is byte addressable.

### Pipelining

The design must implement pipelining, using a 5 stage MIPS-like pipeline. All pipeline hazards must be handled.

### Program Execution

Regarding these types of instructions, the processor must be able to execute any program written using this instruction set. All RAW and WAR hazards must be handled.

## General Implementation Choices

### Data Forwarding and Hazard Detection

Operand addresses are monitored in each stage so that possible data hazards can be detected during instruction decode. Data forwarding control signals are then assigned where applicable.

### Branch Prediction

Our design implements an assumption of branches being not taken. If the branch is taken, the previous two pipeline registers are flushed and replaced with NOP instructions.

# System

## High Level System Hierarchy Breakdown

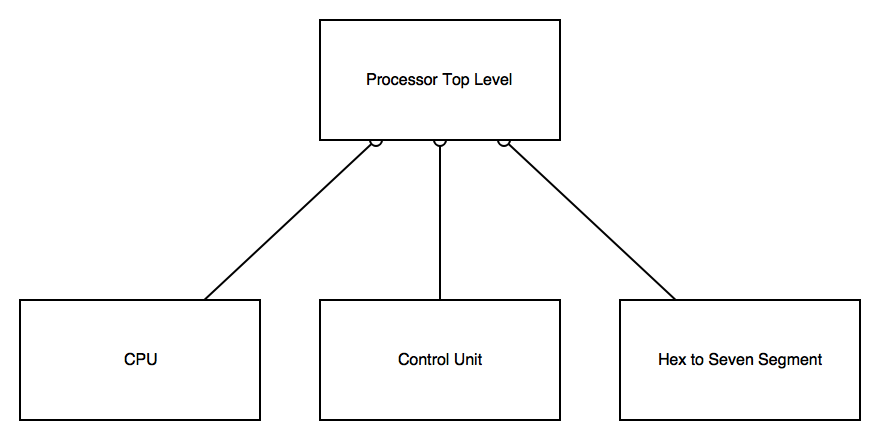


Figure - System Hierarchy Breakdown

The processor is made up of a top-level file connecting the CPU, Control Unit, and Hex to Seven Segment sub-modules together. The CPU module contains its own submodules illustrated in the figure below.

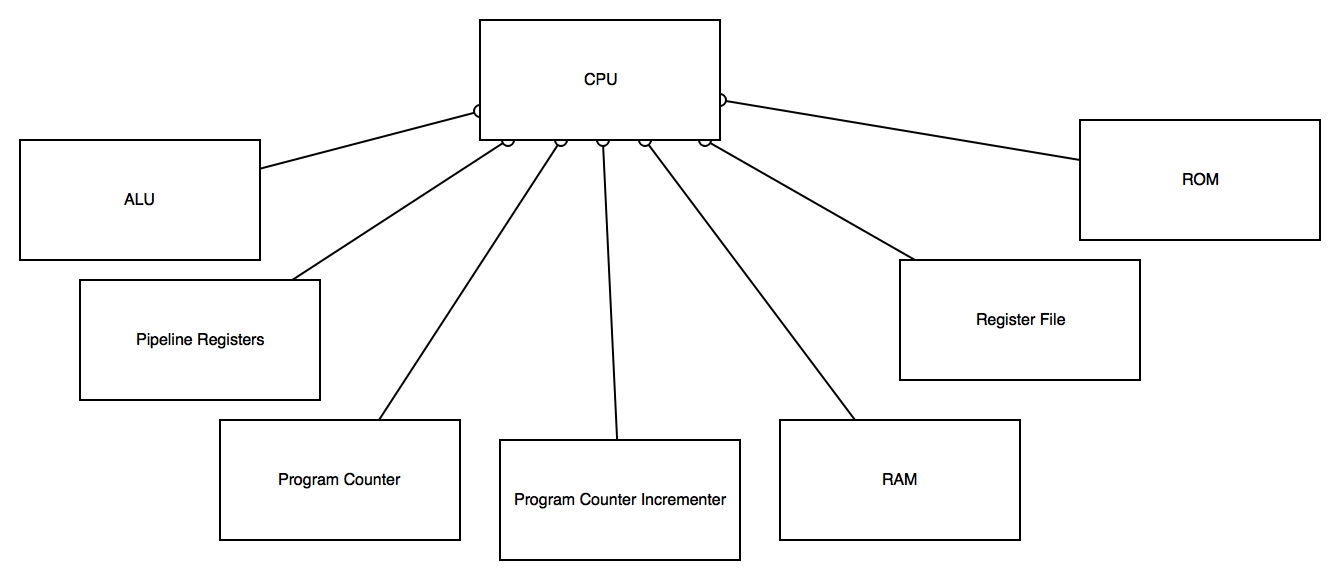


Figure - CPU Hierarchy Breakdown

## High Level System Schematic Breakdown

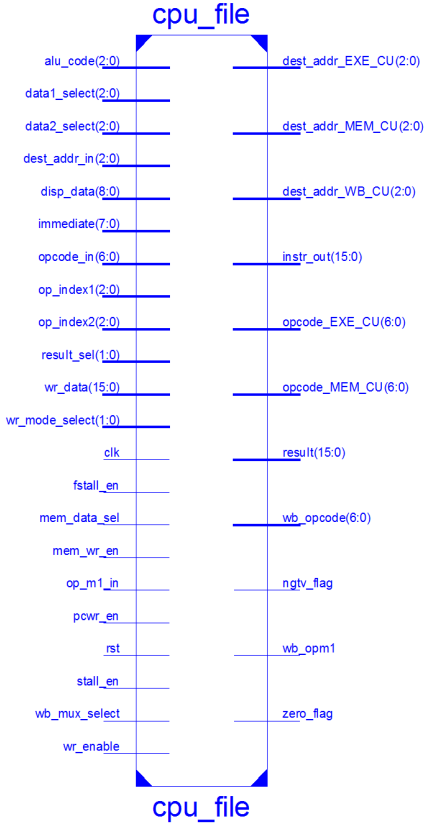


Figure - CPU File RTL Block Schematic

# Individual Module Design

## Top Level Processor Unit

The Top-Level Processor Unit Module handles all connections and routing of the submodules as well as interfacing with the user I/O. The main internal connections connect the Control Unit with the CPU and Hex to Seven Segment Display module.

## CPU

The CPU contains the data path of the processor. Control signals from the control unit implement the instructions read from the program memory. See figure 2 for all submodules contained in the CPU.

### ALU

The ALU executes arithmetic instructions. In the case of multiplication, the ALU will take the 8 LSB’s of both operands and multiply them together for a 16-bit result. The ALU was built to be purely combinatorial resulting in faster execution.

### Multiplexers

Data select signals from the control unit modify the flow of data and addresses based on the needs of the instruction and are used for the implementation of data forwarding.

### Program Counter

The Program counter continually increments through program memory addresses. The count can be held during a stall and branch instructions are able to overwrite the current address value.

### Pipeline Registers

These registers contain the necessary information that is needed by an instruction for the next stage of the pipeline. Information about the instruction that the control unit needs to monitor is also carried forward into the next stage through these registers. The results of the previous stage are written into the register on a falling clock edge and are released into the next stage on a rising clock edge. Reset signals zero out the entire register which effectively replaces the contents with a NOP instruction.

### RAM Module

This is the data memory. Load and store instructions interact with this module.

### ROM Module

This is the program memory and contains the instructions that will be executed by the processor. The program counter sets the address to fetch the instruction from.

### Register File

Contains the 8 general purpose registers used by the processor.

## Control Unit

The design goal for the control unit was to have it be purely combinatorial.

### Data Forwarding and Hazard Detection

Write addresses throughout the pipeline are monitored and compared to the operands of the incoming instruction during decode. A 6-bit code is used to by a process to determine whether a hazard is present and whether to perform data forwarding or a stall.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 5 | 4 | 3 | 2 | 1 | 0 |
| RA | | RB | | RC | |

|  |  |
| --- | --- |
| 00 | No Hazard |
| 01 | Execution |
| 10 | Memory |
| 11 | Write Back |

Based on the current instruction in decode the process checks the code and data forwards from the appropriate stage when possible. For hazards where the data isn’t ready until a later stage stalls are introduced until forwarding can occur. Forwarding is implemented by setting the data select lines or the multiplexers appropriately.

## Hex to Seven Segment Display

The Hex to Seven Segment Display module watches the writeback bus for an output opcode and takes the results from the bus and decodes them for use on the seven segment display.

# Simulation Result

## Format A Instructions

## Format B Instructions

## Format L Instructions

# Analysis and Discussion

## Hardware Verification Procedures

# Conclusion

# Appendices

## VHDL Code

### All VHDL Code available at

### https://github.com/HansSanitizer/CENG-450-Project/tree/master/processor

## RTL Schematics

### Processor Top Level Schematic

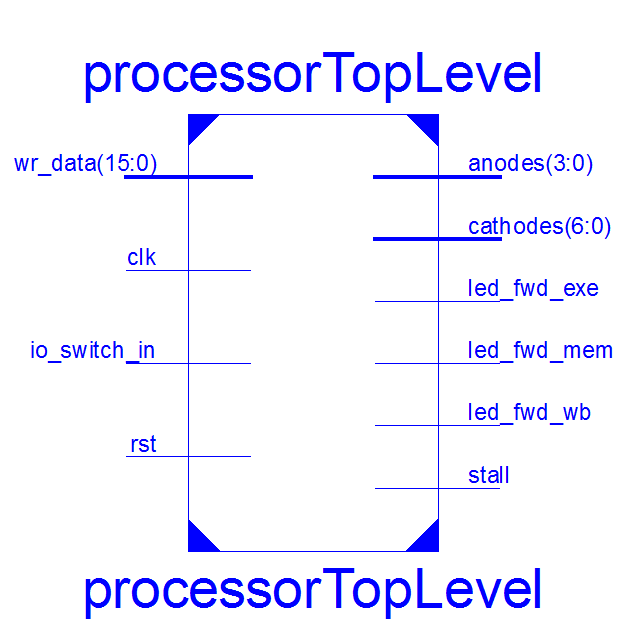


Figure - Processor Top Level Schematic

### Processor Internal Connections

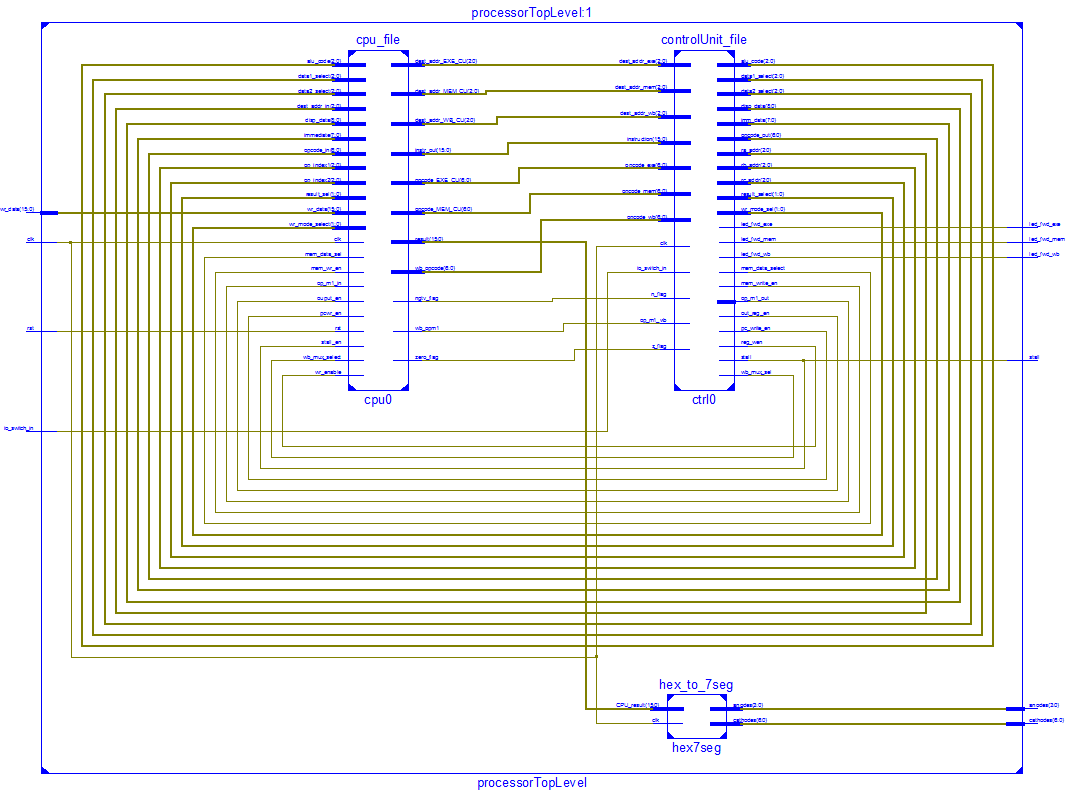


Figure - Processor Internal Connections

### CPU File Top Level Schematic

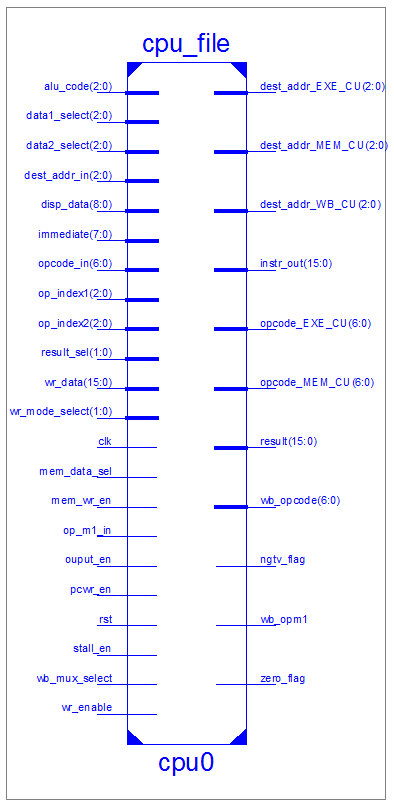


Figure - CPU Top Level Schematic

### CPU Internal Connections

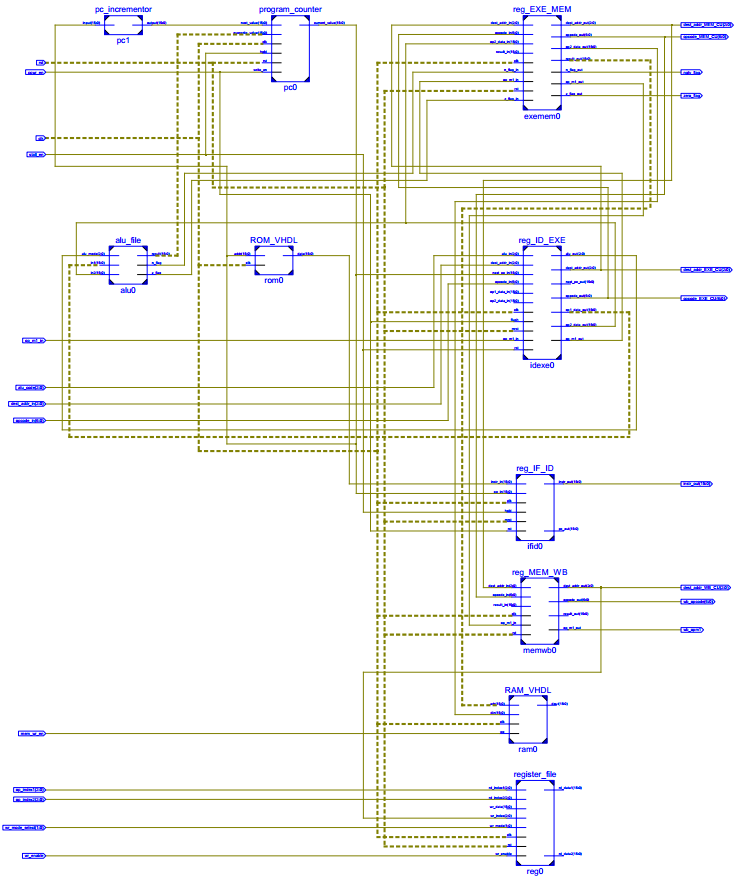


Figure - CPU Internal Connections (MUX's Omitted)

### CPU Pipeline Stages

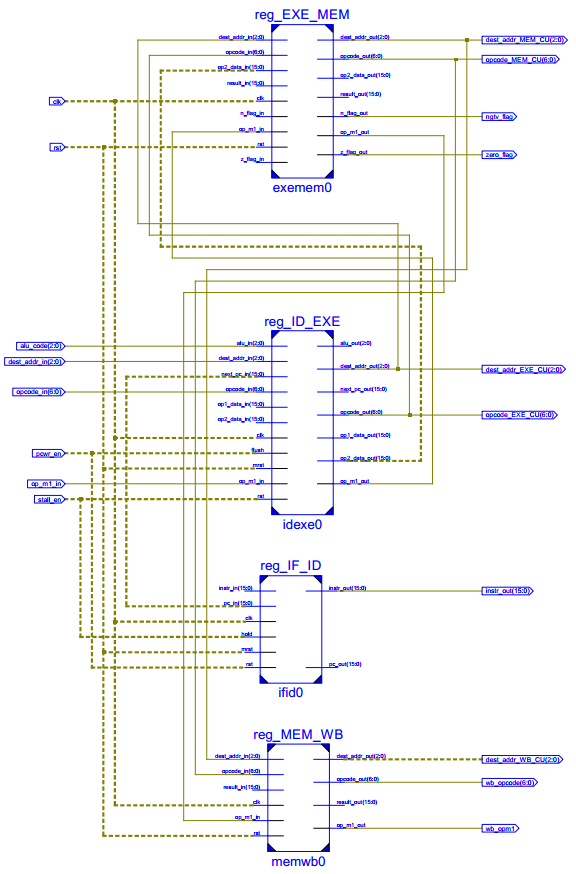


Figure - Pipeline Stages Connection Schematic

### Control Unit Top Level Schematic

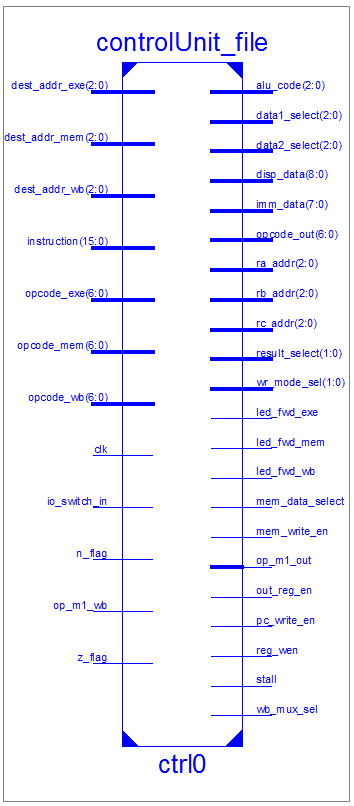


Figure - Control Unit Top Level Schematic