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|  | 16-bit Five Stage MIPS Processor |
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# Objective

## Abstract

Modern processors implement pipelining to increase throughput. Many current processors implement pipelining with various stage depths having more than 5 stages such as Intel, AMD, and even current ARM processors. Pipelining is a standard across all modern architecture designs.

## Project Objective

Build a processor; using VHDL to describe the processor, and Xilinx to synthesize and implement the design on a Spartan 3E FPGA.

# Design Requirement

## General Design Requirements

### Instruction Set

The project must implement a 16-bit RISC-like instruction set. Following the format outlined on the lab website. (Dimopolous & Hazmi, 2017) The instructions are all 1-word long.

The processor must handle three types of instructions:

* A-Format (arithmetic instructions)
* B-Format (branch instructions)
* L-Format (load and store instructions)

### Registers and Memory

Registers and Memory require certain implementations:

* 8 16-bit general purpose registers, each 1-word long, with word alignment.
* A memory address space that is byte addressable.

### Pipelining

The design must implement pipelining, using a 5 stage MIPS-like pipeline. All pipeline hazards must be handled.

### Program Execution

Regarding these types of instructions, the processor must be able to execute any program written using this instruction set. All RAW and WAR hazards must be handled.

## General Implementation Choices

# System

## System Hierarchy Breakdown

## System Schematic Breakdown

# Individual Module Design

## Top Level Processor Unit

## CPU

### ALU

### Muxes

### Program Counter

### Pipeline Registers

### RAM Module

### ROM Module

### Register File

## Control Unit

# Simulation Result

## Simulation Procedures

* Add, then Sub, Then Mul, Then Divide

# Analysis and Discussion

## Hardware Verification Procedures

# Conclusion

# Appendices

# References